REMARKS

Claims 1-20 are pending. Claims 1-2, 8 and 11 have been amended. In view of the following, all pending claims are in condition for allowance. If, after considering this response, the Examiner does not agree that all of the claims are allowable, he is requested to schedule a teleconference with the Applicants' attorney to further the prosecution of the application.

Objection to claims 2 and 11

Claims 2 and 11 have been amended to overcome this objection.

Rejection of claims 1-8 under 35 U.S.C. §112, second paragraph

Claim 1

Claim 1 recites a first means for turning off the switch with a turn-off delay, and a second means for turning on the switch with a turn-on delay shorter than the turn-off delay.

For example, referring, *e.g.*, to FIG. 4 and paragraphs 53-61 of the present application, a first means 88 turns off the switch 81 with a turn-off delay, and a second means 86 turns on the switch 81 with a turn-on delay shorter than the turn-off delay (because resistor 86 has a smaller value than resistor 88). Therefore, there is adequate disclosure showing what is meant by "second means" in claim 1.

Claims 2-8

Claims 2-8 are patentable by virtue of their dependencies from claim 1.

Rejection of claims 1 and 3-5 under 35 U.S.C. §102(b) as being anticipated by Pechlaner et al. (DE 199 28 760)

Claim 1

Claim 1 recites a device for protecting a circuit against a polarity reversal, the device comprising a controllable switch interposed between a first terminal of a DC power supply and a first terminal of the circuit.

For example, referring, *e.g.*, to FIG. 4 and paragraphs 53-61 of the present application, a device 8 protects a circuit 1 against a polarity reversal. The device 8 comprises a controllable switch 81 interposed between a first terminal 32 of a DC power supply Vbat and a first terminal 14 of the circuit 8.

Pechlaner, on the other hand, does not disclose a device for protecting a circuit against a polarity reversal, the device comprising a controllable switch interposed between a first terminal of a DC power supply and a first terminal of the circuit. The Examiner interprets the intelligent semiconductor switch 5 of Pechlaner as the "controllable switch" on page 3 of the Office Action. However, the intelligent semiconductor switch 5 is simply interposed between the first power supply terminal 1 and the ground terminal GND. Or in the alternative, the intelligent semiconductor switch 5 is simply interposed between the first power supply terminal 1 and the load 11, which is connected to the second power supply terminal 2 (page 8 of Pechlaner clearly lists terminals 1 and 2 as first and second power supply terminals for Vbb). Either way, the intelligent semiconductor switch 5 is not interposed between a first terminal of the DC power supply and a first terminal of the circuit that it is protecting. Not only does the intelligent semiconductor switch 5 not protect the ground GND, the load 11, or the power supply Vbb against a polarity reversal, but none of these elements are even a "circuit" as recited in claim 1 of the present application. Therefore, Pechlaner does not satisfy the limitations of claim 1.

Claims 3-5

Claims 3-5 are patentable by virtue of their dependencies from claim 1.

Rejection of claims 2 and 6-8 under 35 U.S.C. §103(a) as being unpatentable over Pechlaner

Claims 2 and 6-8 are patentable by virtue of their dependencies from claim 1.

Rejection of claims 9-20 under 35 U.S.C. §103(a) as being unpatentable over Pechlaner in view of Yamada et al. (US 5,726,505)

Claim 9

Claim 9 recites a switch operable to conduct a current to a first node of a power supply when the first node has a predetermined polarity relative to a second node of the power supply, and a first delay coupled to the switch and operable to disable the switch from conducting current at a predetermined time after the polarity reverses.

For example, referring, *e.g.*, to FIGS. 2 and 4 of the present application, a switch 81 is operable to conduct a current to a first node 32 of a power supply Vbat when the first node 32 has a predetermined polarity relative to a second node 31 of the power supply Vbat. A first delay (82, 88) is coupled to the switch 81 and is operable to disable the switch 81 from conducting current at a predetermined time after the polarity reverses. It should be noted that the first delay (82, 88) is a physical part of the circuit that can disable another physical part 81 of the circuit. It should be further noted that a polarity reversal of the power supply Vbat must first be detected, and then after a predetermined time, the first delay (82, 88) disables the switch 81.

Pechlaner, on the other hand, does not teach a switch operable to conduct a current to a first node of a power supply when the first node has a predetermined polarity relative to a second node of the power supply, and a first delay coupled to the switch and operable to disable the switch from conducting current at a predetermined time after the polarity reverses. The Examiner interprets the semiconductor switch 3 of Pechlaner as the "switch" and the signal delay between control device 4 and the switch 3 as the "first delay" on page 6 of the Office Action. However, the signal delay between the control device 4 and the switch 3 is simply a measure of time. This time measurement is nothing more than a number. The "first delay" recited in claim 9 of the present application is actually a physical part of the circuit that disables the switch after a reverse in polarity is detected. A number cannot do this. Furthermore, the Examiner concedes on page 6 of the Office Action that Pechlaner fails to describe any of the circuitry within the control device 4. As a result, not only does Pechlaner fail to teach any circuitry within the control device 4 to disable the switch 3 after a polarity reversal, but Pechlaner fails to teach any circuitry within the control device 4 to disable the switch 3 at a predetermined time after a polarity reversal.

Similarly, Yamada does not teach any of the shortcomings of Pechlaner. Instead, Yamada teaches a current detector 6 that detects a current flowing from a solar

power supply 1 to a battery power supply 2 (FIGS. 1-2). If this current flowing from the solar power supply 1 to the battery power supply 2 falls below a certain level, the current detector 6 opens MOSFET 5 to prevent current from ever flowing from the battery power supply 2 to the solar power supply 1 (col. 5, lines 19-56). However, this all has nothing to do with the polarity reversal of a single power supply. Neither the solar power supply 1 nor the battery power supply 2 ever reverses polarity. Both the solar power supply 1 and the battery power supply 2 always maintain their polarity, only the amount of current that flows from the solar power supply 1 to the battery power supply 2 changes (the direction of this current does not change because of MOSFET 5). As a result, not only does Yamada fail to teach any circuitry to disable a switch at a predetermined time after a polarity reversal, but Yamada fails to teach any kind of power supply polarity reversal whatsoever.

Therefore, not only is there no motivation to combine the teachings of Pechlaner and Yamada, but the combination of Pechlaner and Yamada does not even satisfy the limitations of claim 9.

Claims 13, 17-18 and 20

Claims 13, 17-18 and 20 are patentable for reasons similar to those recited above in support of the patentability of claim 9.

Claims 10-12, 14-16 and 19

Claims 10-12, 14-16 and 19 are patentable by virtue of their respective dependencies from claims 9, 13 and 18.

CONCLUSION

In light of the foregoing, claims 1-20 are in condition for allowance, which is respectfully requested.

If, after considering this response, the Examiner does not agree that all of the claims are allowable, then it is respectfully requested that the Examiner schedule a phone interview with the Applicants' attorney at (425) 455-5575.

Dated this 4th day of June, 2007.

Respectfully submitted,

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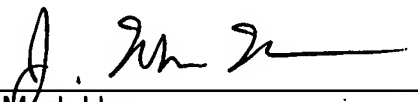

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